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| 10/527,098 | 03/09/2005 | Rob Anne Beuker | NL02 0815 US | 3804 |

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| EXAMINER | |
|---|---|
| MA, TIZE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2628 | |

| NOTIFICATION DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/527,098 | BEUKER, ROB ANNE | |
| | Examiner | Art Unit | |
| | TIZE MA | 2628 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 5-7 are objected to because of the following informalities:

The phrase "any one of the claim 2" should be just "claim 2".

Appropriate correction is required.

2. Claim 6 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

### *Claim Rejections - 35 USC § 101*

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 6-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

5. Regarding claim 6, the claimed invention is directed to an algorithm, which is failing to be limited to embodiments which fall within a statutory category.

6. Regarding claim 7, the claimed invention is a computer program. A computer program without a computer readable medium is not a physical "thing". Therefore a computer program per se, although it can be functional descriptive materials, is not statutory.

7. Regarding claim 8, the claimed invention is an information carrier. An information carrier is interpreted as an electromagnetic signal. The electromagnetic signal is form of

energy. It does not appear that a claim reciting a signal encoded (carried) with functional description materials falls within any of the categories of patentable subject matter set forth in 35 U.S.C. 101.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al (US 5,587,962), and in view of Hackett et al (US 5,585,863).

10. Regarding claim 1, Hashimoto et al teaches a method of operating a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) , wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer (address sequencers 40a and 40b in Fig. 2), each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line (address generators 28a and 28b in Fig. 2) , characterized in that switching means operate the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from [a block of] line pointers in address table register means with the output of pixel counting means, and in a second

mode wherein [a block of] line pointers from a full table of line pointers in said memory is downloaded into said address table register means (Fig. 3 and column 4, lines 8-11. Two modes of operations, the random access mode and the serial mode. The random access mode is the same as the first mode in the instant claim, and the serial mode is the same as the second mode).

11. However, Hashimoto et al generates the memory addresses of the line pointers for the entire frame. That is, Hashimoto et al does not teach the operations based on a block of line pointers.

12. Hackett et al, in the same field of endeavor, teaches creating a line pointer table for a block of lines (column 2, lines 63-66; column 3, lines 15-20. Horizontally dividing the image into rectangular zones of pixel regions is the same as dividing a frame into blocks of lines) for the related pixel regions of a particular interest. This may also saves memory resources.

13. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method as shown in Hashimoto et al by creating a line pointer table for a block of lines as shown in Hackett et al so that the memory address generations and the memory access modes are based on a block of line pointers for the benefit of saving resources.

14. Regarding claim 2, Hashimoto et al teaches a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) comprising a memory for video data to be displayed (memory 24 in Fig. 2) and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the

video data in said memory (address sequencers 40a and 40b in Fig. 2), characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for line pointers from said table of line pointers, and pixel counting means (address generators 28a and 28b in Fig. 2), the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data (Fig. 3 and column 4, lines 8-11. The random access mode).

15. However, Hashimoto et al does not teach address table register means for a block of line pointers from said table of line pointers and means for successively updating the address table register means with subsequent blocks of line pointers.

16. Hackett et al, in the same field of endeavor, teaches address table register means for a block of line pointers from said table of line pointers and means for successively updating the address table register means with subsequent blocks of line pointers (column 2, lines 63-66; column 3, lines 15-31. Horizontally dividing the image into rectangular zones of pixel regions is the same as dividing a frame into blocks of lines. Also see that the pointer in one table is used to locate other tables) for the related pixel regions of a particular interest. This may also saves memory resources.

17. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit as shown in Hashimoto et al by creating a line pointer table for a block of lines as shown in Hackett et al so that the memory address

generations and the memory access modes are based on a block of line pointers for the benefit of saving resources.

18. Regarding claim 3, Hashimoto et al teaches that switching means are provided by which alternately memory addresses for video data are generated in a first mode in the address sequencer, and in a second mode the address table register is updated with a next block of line pointers (Fig. 3 and column 4, lines 8-11. Two modes of operations, the random access mode and the serial mode. The random access mode is the same as the first mode in the instant claim, and the serial mode is the same as the second mode).

19. Regarding claim 4, Hashimoto et al teaches that the memory comprises a full table of line pointers for different sequences of video data to be displayed (column 5, lines 50-52. Writing addresses generated by the address generator into memory).

20. Claim 5 is rejected based on the same reason as to claim 2 since the driving circuit for display system is always connected to a display system if it is operational.

21. Claims 6-8 are rejected based on the same reason as to claim 2 since they are the software implementation which is necessary to make the circuit in claim 2 operational.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chan (US 6,608,626, for an address generator for display controller making the display scans in both horizontal and vertical modes)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIZE MA whose telephone number is (571)270-3709. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao M. Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tm

/XIAO M. WU/
Supervisory Patent Examiner, Art Unit 2628